North American PCB Military Technology Roadmap

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PCB TECHNOLOGY
ROAD MAPS

RF & Microwave
Handheld - Wireless Ruggedized
Flex Circuits
Roadmap Purpose and Scope

Purpose

• To assist the EA, leading North American printed board manufacturers of the IPC EA Task Force created this roadmap, which identifies the challenging printed board designs and materials that will be required to meet future DoD and OEM needs.
• The task force believes this roadmap can facilitate better communication between:
  - The printed board industry
  - OEMs designing and manufacturing military hardware;
  - DoD and the military electronics supply chain.
• The electronics industry would benefit from a more complete understanding of current and future DoD/OEM needs particularly in the areas of critical parts, materials and designs.

Scope of the IPC Defense Roadmap (IPC/DR)

• Identifies and addresses the challenging printed board designs, production processes and materials required to meet future DoD and OEM needs for 2009 and 2010.
• Identifies anticipated advances in technology that require gap-filling.
• The roadmaps are not a replacement or amendment to the IPC International Technology Roadmap for Electronic Interconnections.
IPC PCB Defense Roadmaps

**Introductions**

- **RF & Microwave**
  - George Dudnikov - Sanmina

- **Ruggedized Handheld & Wireless**
  - Andy Cameron - TTM Technologies

- **Flex and Rigid Flex**
  - Al Wasserzug - Vulcan Flex Circuit
IPC Printed Circuit Board
Defense Roadmap
IPC/DR

PCB Materials and Technology
for RF Microwave Applications

George Dudnikov
Sanmina - SCI
Radio Frequency (RF)

Radio Frequency

Infrared
Visible
Ultraviolet
X-Ray
Gamma-Ray
Cosmic-Ray

1 MHz
1 GHz
1 THz

1 KHz
10 KHz
100 KHz
1 MHz
10 MHz
100 MHz
1 GHz
10 GHz
100 GHz
1 THz

VLF
LF
MF
HF
VHF
UHF
SHF
EHF

Microwaves

L
S
C
X
Ku
K
Ka
V
W

Cell Phones
WIFI (L5)
Bluetooth
WIFI (HS)

IPC Member
# RF and Microwave Roadmap

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Printed Board Materials</td>
<td>Very Low loss</td>
<td>Very Low loss</td>
<td>Very Low loss</td>
<td>Very Low loss</td>
<td>New materials being developed every three to six months</td>
</tr>
<tr>
<td></td>
<td>Low Dk</td>
<td>Low Dk</td>
<td>Low Dk</td>
<td>Low Dk</td>
<td>Improve weight and performance</td>
</tr>
<tr>
<td></td>
<td>Light weight</td>
<td>High Dk</td>
<td>High Dk</td>
<td>Foams</td>
<td>Need testing on plateability and reliability</td>
</tr>
<tr>
<td>Max Board Size (mm)</td>
<td>300x400</td>
<td>1220x1420</td>
<td>300x400</td>
<td>1220x1420</td>
<td>Emerging technologies for lamination, plating and conductive pastes</td>
</tr>
<tr>
<td>Board Thickness (mil)</td>
<td>1.5–2.5</td>
<td>7.5</td>
<td>1.5–4.0</td>
<td>10.0</td>
<td>Material testing required</td>
</tr>
<tr>
<td>Number of Lamination Cycles</td>
<td>1–2</td>
<td>1–6</td>
<td>1–3</td>
<td>1–6</td>
<td>Mixing different Dk materials and foams</td>
</tr>
<tr>
<td>Number of Different Materials</td>
<td>1–2</td>
<td>1–4</td>
<td>1–3</td>
<td>1–6</td>
<td>Reliability of RF and digital on same board with different materials is unknown</td>
</tr>
<tr>
<td>Maximum Layer Count</td>
<td>12</td>
<td>36</td>
<td>16</td>
<td>40</td>
<td>Fine lines/spaces on digital side of mixed technology product</td>
</tr>
<tr>
<td>Minimum L/S Internal (µm)</td>
<td>125/125</td>
<td>75/75</td>
<td>75/75</td>
<td>60/50</td>
<td>Fine lines/spaces on digital side of mixed technology product</td>
</tr>
<tr>
<td>Minimum L/S Plated Layers (µm)</td>
<td>125/125</td>
<td>75/75</td>
<td>100/100</td>
<td>75/75</td>
<td>Fine lines/spaces on digital side of mixed technology product</td>
</tr>
<tr>
<td>Minimum Drill Diameter Thru Via (µm)/Aspect Ratio</td>
<td>300</td>
<td>260</td>
<td>200</td>
<td>150</td>
<td>Fine lines/spaces on digital side of mixed technology product</td>
</tr>
<tr>
<td>Hole Quantity</td>
<td>11,000</td>
<td>14,000</td>
<td>13,000</td>
<td>16,000</td>
<td>Fine lines/spaces on digital side of mixed technology product</td>
</tr>
<tr>
<td>Minimum Via Drill Ene/Blind</td>
<td>250</td>
<td>200</td>
<td>200</td>
<td>150</td>
<td>Fine lines/spaces on digital side of mixed technology product</td>
</tr>
<tr>
<td>Hole Quantity</td>
<td>2,000</td>
<td>4,000</td>
<td>4,000</td>
<td>6,000</td>
<td>Fine lines/spaces on digital side of mixed technology product</td>
</tr>
<tr>
<td>Minimum Microvia Laser Diameter (µm)/Aspect Ratio</td>
<td>250</td>
<td>150</td>
<td>150</td>
<td>100</td>
<td>Fine lines/spaces on digital side of mixed technology product</td>
</tr>
<tr>
<td>µVia Quantity</td>
<td>1,000</td>
<td>5,000</td>
<td>5,000</td>
<td>20,000</td>
<td>Fine lines/spaces on digital side of mixed technology product</td>
</tr>
<tr>
<td>Hole-to-Cu Keep Out (µm)</td>
<td>500</td>
<td>375</td>
<td>375</td>
<td>200</td>
<td>Fine lines/spaces on digital side of mixed technology product</td>
</tr>
<tr>
<td>Soldier Mask Registration DTP (µm)</td>
<td>100</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>Fine lines/spaces on digital side of mixed technology product</td>
</tr>
</tbody>
</table>

*Note: All information is subject to change and may not be applicable to all applications.*
Key PCB Technology Drivers for RF and Microwave

- Low Dielectric Low Loss Laminate materials
- Mixed Signal Applications: Digital / RF on same PCB
- Composite Stackups: Multiple materials in same card
- Drilling and Plating of Teflon based materials
- RF elements requiring tight lithography/etch controls
- Microvias and Plated Over Filled Vias
- Embedded Passives (R,C & L)
- Thermal Management Solutions
- High Reliability Assessment
- Test and Measurement
Advanced PCB Technologies for RF and Microwave

Micro Via Hole Laser Drill Technology

Hole Metallization Plating Technology

PPR Plating High Aspect

Embedded Passives ZBC™ Technology Buried Resistors

Fine Pattern Process Technology

Subcomposite Via Hole Buried Vias Via Filling

High Performance Materials Composite Constructions

Computer Aided Engineering Simulation Technology
### RF Dielectric Materials

<table>
<thead>
<tr>
<th>Brand</th>
<th>Part</th>
<th>Resin</th>
<th>Dk</th>
<th>Df</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nelco</td>
<td>N4000-8FC</td>
<td>FR-4</td>
<td>4.2</td>
<td>0.023</td>
</tr>
<tr>
<td></td>
<td>N4000-12</td>
<td>Modified FR-4</td>
<td>3.6</td>
<td>0.008</td>
</tr>
<tr>
<td></td>
<td>N4000-12SL</td>
<td>Modified FR-4</td>
<td>3.3</td>
<td>0.007</td>
</tr>
<tr>
<td></td>
<td>N4000-13</td>
<td>Modified FR-4</td>
<td>3.6</td>
<td>0.008</td>
</tr>
<tr>
<td></td>
<td>N4000-13CI</td>
<td>Modified FR-4</td>
<td>3.3</td>
<td>0.007</td>
</tr>
<tr>
<td></td>
<td>N6000-32</td>
<td>BT Epoxy</td>
<td>4.1</td>
<td>0.009</td>
</tr>
<tr>
<td></td>
<td>N7000-1</td>
<td>Non-MDA Polymide</td>
<td>3.7</td>
<td>0.007</td>
</tr>
<tr>
<td>Isola</td>
<td>FR409</td>
<td>Modified FR-4</td>
<td>3.63</td>
<td>0.013</td>
</tr>
<tr>
<td></td>
<td>IS620</td>
<td>BT/CE</td>
<td>3.59</td>
<td>0.010</td>
</tr>
<tr>
<td></td>
<td>IS640</td>
<td>BT/CE</td>
<td>3.45</td>
<td>0.005</td>
</tr>
<tr>
<td></td>
<td>P96</td>
<td>Polyimide</td>
<td>4.01</td>
<td>0.022</td>
</tr>
<tr>
<td>Isola-Polyclad</td>
<td>Getek ML200D</td>
<td>Polyphenylene Ether (PPE)</td>
<td>3.5</td>
<td>0.010</td>
</tr>
<tr>
<td>Arlon</td>
<td>25N</td>
<td>Ceramic Hydrocarbon</td>
<td>3.38</td>
<td>0.0025</td>
</tr>
<tr>
<td></td>
<td>25FR</td>
<td>Ceramic Hydrocarbon</td>
<td>3.59</td>
<td>0.0035</td>
</tr>
<tr>
<td></td>
<td>RO4003C</td>
<td>Ceramic Hydrocarbon</td>
<td>3.38</td>
<td>0.0027</td>
</tr>
<tr>
<td></td>
<td>RO4350B</td>
<td>Ceramic Hydrocarbon</td>
<td>3.48</td>
<td>0.0037</td>
</tr>
<tr>
<td></td>
<td>R/T Duroid 6002</td>
<td>Ceramic-filled PTFE</td>
<td>2.94</td>
<td>0.0012</td>
</tr>
<tr>
<td></td>
<td>R/T Duroid 6006</td>
<td>Ceramic-filled PTFE</td>
<td>6.15</td>
<td>0.0027</td>
</tr>
<tr>
<td></td>
<td>R/T Duroid 6010 LM</td>
<td>Ceramic-filled PTFE</td>
<td>10.8</td>
<td>0.0023</td>
</tr>
<tr>
<td></td>
<td>RO3003</td>
<td>Ceramic-filled PTFE</td>
<td>3.0</td>
<td>0.0013</td>
</tr>
<tr>
<td></td>
<td>RO3006</td>
<td>Ceramic-filled PTFE</td>
<td>6.15</td>
<td>0.0020</td>
</tr>
<tr>
<td></td>
<td>RO3010</td>
<td>Ceramic-filled PTFE</td>
<td>10.2</td>
<td>0.0025</td>
</tr>
<tr>
<td></td>
<td>TMM 3</td>
<td>Ceramic Polymer</td>
<td>3.27</td>
<td>0.0020</td>
</tr>
<tr>
<td></td>
<td>TMM 4</td>
<td>Ceramic Polymer</td>
<td>4.5</td>
<td>0.0020</td>
</tr>
<tr>
<td></td>
<td>TMM 6</td>
<td>Ceramic Polymer</td>
<td>6.0</td>
<td>0.0023</td>
</tr>
<tr>
<td>Rogers</td>
<td>TMM 10</td>
<td>Ceramic Polymer</td>
<td>9.20</td>
<td>0.0022</td>
</tr>
<tr>
<td></td>
<td>TMM 10i</td>
<td>Ceramic Polymer</td>
<td>9.80</td>
<td>0.0020</td>
</tr>
<tr>
<td>Taconic</td>
<td>RF-30</td>
<td>PTFE</td>
<td>3.0</td>
<td>0.0014</td>
</tr>
<tr>
<td></td>
<td>RF-35</td>
<td>PTFE</td>
<td>3.5</td>
<td>0.0019</td>
</tr>
<tr>
<td></td>
<td>RF-35A</td>
<td>PTFE</td>
<td>3.5</td>
<td>0.0025</td>
</tr>
<tr>
<td></td>
<td>TLC</td>
<td>PTFE</td>
<td>3.2</td>
<td>0.0030</td>
</tr>
<tr>
<td></td>
<td>TLX</td>
<td>PTFE</td>
<td>2.5</td>
<td>0.0019</td>
</tr>
<tr>
<td></td>
<td>TLY</td>
<td>PTFE</td>
<td>2.2</td>
<td>0.0009</td>
</tr>
<tr>
<td>W.L.Gore</td>
<td>Speedboard C</td>
<td>PTFE/CE</td>
<td>2.7</td>
<td>0.004</td>
</tr>
<tr>
<td>Hitachi</td>
<td>LX67</td>
<td>Cyanate Ester</td>
<td>3.54</td>
<td>0.0034</td>
</tr>
<tr>
<td>TUC</td>
<td>TU722</td>
<td>Unfilled RoHS FR-4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TI1677</td>
<td>Filled RoHS 180Tg FR-4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TU752</td>
<td>Filled RoHS Hi-Tg FR-4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Many to choose from
- Processing differs and requires development
- Different Electrical Characteristics
- Wide range of Cost
High Frequency Material:
Liquid Crystal Polymer

- Dk = 2.9
- Df = 0.002
- Moisture Absorption = 0.03% by weight
- Adjustable CTE of 17ppm/C and 8 ppm/C (x,y) to match copper or LTCC
- Best barrier properties of a polymer; nearly hermetic
- Thermal Conductivity of 0.5W/mK
  - (FR4 is 0.25W/mK)
- Excellent mm wave frequencies (~ 75 GHz and up)
- Can be used for flex transition layers in R-Flex

<table>
<thead>
<tr>
<th>Laminate</th>
<th>Dk</th>
<th>Df</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCP</td>
<td>2.9 to 3.0</td>
<td>0.002 to 0.003</td>
<td>100% resin</td>
</tr>
<tr>
<td>Ultralam 2000</td>
<td>2.4 to 2.6</td>
<td>0.0022 max</td>
<td>Woven glass reinforced PTFE</td>
</tr>
<tr>
<td>RO4003/RO4350</td>
<td>3.38/3.48</td>
<td>0.0024/0.0034</td>
<td>Glass reinforced ceramic filled thermoset</td>
</tr>
<tr>
<td>RO4232</td>
<td>3.2</td>
<td>0.0018</td>
<td></td>
</tr>
<tr>
<td>RO3203/3206/3210</td>
<td>3.02/6.15/10.2</td>
<td>.0016/.0027/.0027</td>
<td>Glass, ceramic and reinforced thermoset</td>
</tr>
<tr>
<td>RT Duroid</td>
<td>2.2-2.3</td>
<td>0.0004-0.0012</td>
<td>Glass microfiber -PTFE</td>
</tr>
</tbody>
</table>
Hybrid or Composite Construction

Hybrid construction typically involve a low loss material such as N4000-13, FR408, Rogers 4350, Taconic RF35 combined with another core material. The low loss material is typically placed on the outer layers, but in some case can be a sub-assembly.

Electrical performance is maintained at a reduced cost.
Hybrid Construction Examples

Taconic RF35A + PCLFR370HR

N4000-7SI

N4000-6SI

N4000-7SI
Hybrid Construction Constructions

Rogers RO4350B + N4000-13 Hybrid

Rogers RO4003 + FR406 Hybrid
Etch defined Surface  RF Structures

RF elements require:
• Precision Imaging Controls
• Tightly Controlled Etching Process Tolerances
Edge Plating for EMI Shielding

Without Edge Plating:
Excessive Radiation

With Edge Plating:
Excessive Radiation is Contained

Note Via Fencing Around Route Tab
Circuit Isolation Using Via Fencing

Single Row

Double Row For Increased Isolation
Complex RF Power Divider Networks using PTF Buried Resistors

- Complex Wilkinson Power Divider Network for RF Scanning Beam Array Antennas
- Using Low Cost Polymer Thick Film Resistors embedded on internal layers
- Embedded Passives add functionality with reduced space and weight
Thermal Management Solutions

Numerous options exist depending on heat transfer requirements

Options:
- Heavy Copper Internal Planes
- Thermal Vias Plated and/or Filled
- Metal Core
- Copper and Aluminum Heat Spreaders
- Localized Coins
- Embedded, Soldered, Press Fit, Adhesive
- Exotics: Stablcore carbon fiber

Dielectrics:
- Rogers, Arlon, Taconic, Nelco, Gore

Heat Sink Attachment Options:
- Prepreg bonding
- Conductive adhesive
- Sweat soldering
- Cavity Inserts
Metal Backed RF PCB

- Power Amplifier Module
- Attributes:
  - Copper Based Metal Plate
  - Copper heat sink & RF60 PTFE material
  - Controlled Depth Cavity/ Holes reside into the Metal Plate
  - Thick Copper Plate
- Challenges:
  - Mechanical Routing & Drilling to handle both hard Cu & soft PTFE
IPC Printed Circuit Board
Defense Roadmap
IPC/DR

Handheld - Wireless Ruggedized
PCB Technology Road Map

Andy Cameron
TTM Technologies
Handheld - Wireless Roadmap

- **Key Drivers and Focal Points**
  - Fine pitch BGAs and density constraints driving advanced interconnects
  - HDI enabling capabilities
  - Robust lead free materials

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical Board Size (mm)</td>
<td>50x150</td>
<td>38x100</td>
<td>36x100</td>
<td>25x75</td>
<td>- A significant increase of commercialization is moving to lead-free</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>- Historic lead-free printed boards may make FR-4 obsolete</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>- Material testing is required</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>- Moisture uptake and brittle nature</td>
</tr>
<tr>
<td>Typical Board Thickness (mm)</td>
<td>0.75 ± 0.157</td>
<td>0.75 ± 0.157</td>
<td>0.75 ± 0.157</td>
<td>0.75 ± 0.157</td>
<td>- Use of thinner cores and prepress</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>- Higher reliability requires testing</td>
</tr>
<tr>
<td>Number of Elimination Cycles</td>
<td>1-2</td>
<td>1-4</td>
<td>1-4</td>
<td>1-6</td>
<td>- Reliability requirements for speed and technology</td>
</tr>
<tr>
<td>Number of Types</td>
<td>8</td>
<td>12</td>
<td>8</td>
<td>10</td>
<td>- Requires a maximum of 1/2 oz copper</td>
</tr>
<tr>
<td>Maximum Lead Count</td>
<td>8</td>
<td>12</td>
<td>8</td>
<td>10</td>
<td>- Requires improved small hole plating methods</td>
</tr>
<tr>
<td>Minimum Plated (µm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>All layers that have microvias require plating, new dry films, plating</td>
</tr>
<tr>
<td>Maximum plated (µm)</td>
<td>200</td>
<td>180</td>
<td>180</td>
<td>180</td>
<td>and planarization methods</td>
</tr>
<tr>
<td>Minimum plated (µm)</td>
<td>9,1</td>
<td>10.1</td>
<td>10.1</td>
<td>10.1</td>
<td>- New materials, movement testing, registration and Low Density</td>
</tr>
<tr>
<td>Hole Diameter (µm)</td>
<td>1500</td>
<td>1000</td>
<td>2000</td>
<td>1500</td>
<td>Interconnect systems</td>
</tr>
<tr>
<td>Minimum plated (µm)</td>
<td>200</td>
<td>150</td>
<td>150</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Minimum plated (µm)</td>
<td>785</td>
<td>3643</td>
<td>895</td>
<td>3817</td>
<td>Providing improved small hole plating methods</td>
</tr>
<tr>
<td>Hole-to-Cu Keep Out (µm)</td>
<td>250</td>
<td>200</td>
<td>200</td>
<td>250</td>
<td></td>
</tr>
<tr>
<td>Solder Mask Registration</td>
<td>100</td>
<td>75</td>
<td>76</td>
<td>60</td>
<td>- Improved solder mask methods needed</td>
</tr>
<tr>
<td>Diameter True Position (µm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>- As Low Density Interconnect systems</td>
</tr>
</tbody>
</table>
Fine-Pitch BGA Implications

Conventional Mechanically Drilled Through Vias

- 1.00mm = 39.4 mils pitch
- 0.80mm = 31.4 mils pitch

### Annular Ring Requirements Class 2 or 3

<table>
<thead>
<tr>
<th>Package Pitch</th>
<th>Pad Size</th>
<th>Laser Size</th>
<th>Trace Size</th>
<th>Space</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>μm</td>
<td>mils</td>
<td>μm</td>
<td>mils</td>
</tr>
<tr>
<td>0.65 MM</td>
<td>356</td>
<td>14.0</td>
<td>152</td>
<td>6.0</td>
</tr>
<tr>
<td>0.50 MM</td>
<td>254</td>
<td>10.0</td>
<td>114</td>
<td>4.5</td>
</tr>
<tr>
<td>0.40 MM</td>
<td>216</td>
<td>8.5</td>
<td>102</td>
<td>4.0</td>
</tr>
<tr>
<td>0.35 MM</td>
<td>191</td>
<td>7.5</td>
<td>89</td>
<td>3.5</td>
</tr>
<tr>
<td>0.30 MM</td>
<td>167</td>
<td>6.6</td>
<td>76</td>
<td>3.0</td>
</tr>
<tr>
<td>0.25 MM</td>
<td>127</td>
<td>5.0</td>
<td>64</td>
<td>2.5</td>
</tr>
</tbody>
</table>

Center of Gravity
- .65-.50mm
- State of the Art .40mm and below

States of the Art 40mm and below
Example Interconnect Structure

- Handheld communication device
- 3+N+3 stacked and staggered micro-vias
- .50mm pitch device escape routing drove interconnect use
- Multiple lamination, drilling, plating and imaging cycles
Fine-Pitch BGA Enablers

- Laser drilling capabilities for 75-150µm holes
- Fine line imaging and etching capabilities for inner layers and plated layers
- Improved plating processes targeted at flexibility for numerous metallization requirements
- Robust laser drillable dielectric materials that are lead free capable and can be used in hybrid RF-digital applications
Fine-Pitch BGA Drill & Imaging

- Laser drilling of holes 75-150µm in diameter
  - Glass reinforced or homogenous dielectrics
  - Aspect ratios of 0.5:1 to 1.0:1 typically
  - UV Yag, CO\textsuperscript{2} and/or combination ablation systems

- Laser Direct Imaging vs. plotted film printing needed at various process stages to meet the registration and resolution requirements:
  - Internal Layers
  - External and Plated Sub Laminations
  - Soldermask

50 µm line
Plating Developments

• Advanced plating capability focus:
  - Small, high aspect ratio mechanical drilled through holes and buried vias (100µm - 200µm)
  - Minimizing surface layer plating thickness to open the window for fine line and space requirement on layers requiring multiple plating cycles (wrap plating)
  - Pad surface flatness requirements for via in pad
  - Copper filling, conductive or non conductive fill of microvias or other means required for stacking of fine pitch array structures
  - Improved flexibility and efficiency providing reduced cycle times
### Robust Lead Free Materials

- **Lead Free material challenges**
  - Naturally occurring moisture levels and lead-free temperatures combine to double the vapor pressure within the PCB
  - Delamination risk increases at lead-free assembly temperatures - may not be evident on the surface
  - Design points, thicker product and tighter hole to hole spacing can make delamination more prevalent
  - Lead free resin systems are generally more brittle in nature and require additional process optimization
  - Product requiring multiple lamination cycles degrades the materials resilience to further thermal excursions in 245-260 C
Handheld-Wireless & Ruggedized Summary

- Continued lead free laminate development and reliability testing is crucial based on its foundational position within all electronics platforms.
- The application of fine pitch BGAs to PCBs in significant volumes requires advanced equipment, materials and methods to provide acceptable yield, cost, scalability and reliability.
- Transitioning to HDI interconnects with lead free soldering for Defense applications is complex but is achievable today.
IPC Printed Circuit Board
Defense Roadmap
IPC/DR

Flex Circuit
Technology Road Map

Al Wasserzug
Vulcan Flex Circuit Corporation
# Flex Circuit Roadmap

<table>
<thead>
<tr>
<th>Attribute</th>
<th>2009 RCG</th>
<th>2009 SoA</th>
<th>2010-2011 RCG</th>
<th>2010-2011 SoA</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Materials</td>
<td>copper, polyimide films, acrylic adhesive,</td>
<td>copper, polyimide films, acrylic adhesive,</td>
<td>copper, polyimide films, acrylic adhesives,</td>
<td>copper, polyimide films, acrylic adhesive,</td>
<td>Thermal management, signal integrity and dimensional stability are issues</td>
</tr>
<tr>
<td></td>
<td>polyimide glass, epoxy glass and associated</td>
<td>polyimide glass, epoxy glass and associated</td>
<td>polyimide glass, epoxy glass, PTFE and</td>
<td>polyimide glass, epoxy glass, PTFE and</td>
<td></td>
</tr>
<tr>
<td></td>
<td>pre-pregs</td>
<td>pre-pregs</td>
<td>associated pre-pregs</td>
<td>associated pre-pregs</td>
<td></td>
</tr>
<tr>
<td>Board (Panel) Size (mm)</td>
<td>456.9 mm X 609.1 mm (18&quot; X 24&quot;)</td>
<td>609.1 mm X 761.4 mm (24&quot; X 30&quot;)</td>
<td>609.1 mm X 761.4 mm (24&quot; X 30&quot;)</td>
<td>761.4 mm X 913.7 mm (24&quot; X 36&quot;)</td>
<td>Panel fabrication only</td>
</tr>
<tr>
<td>Board Thickness (mm)</td>
<td>4.75 mm (.187&quot;)</td>
<td>6.35 mm (.250&quot;)</td>
<td>6.35 mm (.250&quot;)</td>
<td>&gt; 6.35 mm (.250&quot;)</td>
<td>Minimum dielectric required</td>
</tr>
<tr>
<td>Number of Lamination Cycles</td>
<td>2 cycles</td>
<td>&gt; 3 cycles</td>
<td>3 cycles</td>
<td>&gt; 4 cycles</td>
<td><strong>&quot;crossing legs&quot;</strong> adds to complexity</td>
</tr>
<tr>
<td>Number of Material Types (Mixed Stack Up)</td>
<td>3</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>Other can be cuprous-nickel, ITO, constantan, beryllium copper, and exotic dielectrics</td>
</tr>
<tr>
<td>Layer Count</td>
<td>16</td>
<td>&gt; 16</td>
<td>20</td>
<td>&gt; 24</td>
<td>½ oz. copper</td>
</tr>
<tr>
<td>Minimum line/space internal (µm)</td>
<td>102 µm (.004&quot;)</td>
<td>76 µm (.003&quot;)</td>
<td>76 µm (.003&quot;)</td>
<td>51 µm (.002&quot;)</td>
<td>1 oz. copper</td>
</tr>
<tr>
<td>Minimum line/space plated layers (µm)</td>
<td>127 µm (.005&quot;)</td>
<td>102 µm (.004&quot;)</td>
<td>102 µm (.004&quot;)</td>
<td>76 µm (.003&quot;)</td>
<td></td>
</tr>
<tr>
<td>Minimum Drill diameter via (µm)/</td>
<td>305 µm (.012&quot;)/8:1</td>
<td>254 µm (.010’)/10:1</td>
<td>254 µm (.010’)/10:1</td>
<td>203 µm (.008’)/12:1</td>
<td>May require reverse pulse-plating with aggressive sparging</td>
</tr>
<tr>
<td>Aspect Ratio</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Blind/buried via hole quantity</td>
<td>.03/mm² (3,000/in²)</td>
<td>.05/mm² (5,000/in²)</td>
<td>.05/mm² (5,000/in²)</td>
<td>.07/mm² (7,500/in²)</td>
<td>Only Motherboard type rigid-flexes have many holes</td>
</tr>
<tr>
<td>Minimum Drill diameter buried/blind (µm)</td>
<td>254 µm (.010’)/10:1</td>
<td>228 µm (.009”)</td>
<td>228 µm (.009”)</td>
<td>178 µm (.007”)</td>
<td>Sequential lamination</td>
</tr>
<tr>
<td>Hole Qty</td>
<td>.002/mm² (250/in²)</td>
<td>.004/mm² (500/in²)</td>
<td>.004/mm² (500/in²)</td>
<td>.007/mm² (750/in²)</td>
<td>Conductive via hole fill</td>
</tr>
<tr>
<td>Min microvia laser dia µm/Aspect ratio</td>
<td>102 µm (.004’)/0.5:1</td>
<td>76 µm (.003’)</td>
<td>76 µm (.003’)</td>
<td>51 µm (.002’)</td>
<td>Laser ablated</td>
</tr>
<tr>
<td>Microvia quantity</td>
<td>.002/mm² (250/in²)</td>
<td>.004/mm² (500/in²)</td>
<td>.004/mm² (500/in²)</td>
<td>.007/mm² (750/in²)</td>
<td>Plugged</td>
</tr>
<tr>
<td>Hole-to-Copper keep-out (µm)</td>
<td>254 µm (.010’)</td>
<td>178 µm (.007’)</td>
<td>178 µm (.007’)</td>
<td>152 µm (.006’)</td>
<td>Non-functional pads removed</td>
</tr>
<tr>
<td>Soldermask registration DTP (µm)</td>
<td>76 µm (.003’)</td>
<td>51 µm (.002’)</td>
<td>51 µm (.002’)</td>
<td>38 µm (.0015’)</td>
<td>Soldermask on MB rigid-flex only, Laser Defined Soldermask on rise</td>
</tr>
</tbody>
</table>

*Note: RCG = Rigid Circuit, SoA = Softboard, IPC = Institute of Printed Circuits*
Flex Circuit Roadmap

Key Technology Drivers

• Signal Integrity and Performance
• System/Component Miniaturization
• Space and Weight Reduction
• Handling Issues
• Other Common PCB Features are typical on Rigid-Flex Mother Boards
• Limited Market Limits R&D Investment
Flex Circuit Roadmap

Product Evolutions Supporting Drivers

• Rigid-Flex Circuit Board
  • Backplane
  • Motherboard

• Sculpted Flex Circuit
• Coax & Twisted Shielded Pair emulation
• Oversized Flex Harness (> 36” long)
• Formed-To-Install Flex Circuits
• Chip-On-Flex/TAB/Flip-Chip
Flex Circuit Roadmap

Backplane Type Rigid-Flex Circuit Board in Carrier
Flex Circuit Roadmap
Motherboard Type
Rigid-Flex Circuit Board
Flex Circuit Roadmap

<table>
<thead>
<tr>
<th>* * LAYER * *</th>
<th>* * MATERIAL * *</th>
</tr>
</thead>
<tbody>
<tr>
<td>No.</td>
<td>Designation</td>
</tr>
<tr>
<td>1</td>
<td>Pads Only</td>
</tr>
<tr>
<td>2</td>
<td>2A Power</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>Signals</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>4A Power</td>
</tr>
<tr>
<td>7</td>
<td>Pads Only</td>
</tr>
</tbody>
</table>

Typical Rigid-Flex Cross-Section
Flex Circuit Roadmap

Sculpted Flex Circuit
Flex Circuit Roadmap

Typical Sculpted Flex Circuit Cross-Section

Typical Copper thickness of .010" Nom. in termination areas and fully exposed Finger Patterns.

Copper is Chemically Milled to a thickness of .004" ± .001" in the Circuit Flex area(s).
Flex Circuit Roadmap

Oversized Flex Harness
Cross-Section of Silver Polymer "Stitching" on Typical Rigid-Flex Leg

- Flex Leg Width
- .025" minimum edge of ground trace to edge of Flex Leg

Layer 4
- Copper Conduct
- Internal Dielectric
- Silver Polymer S

Layer 5
- Copper Conduct
- Internal Dielectric

Layer 6
- Copper Conduct
- Internal Dielectric

Layer 7
- Copper Conduct
- Internal Dielectric

Layer 8
- Copper Conduct
- Internal Dielectric
- Silver Polymer S
- Bottom Side Cover

= designates a ground trace. On Layers 4 and 8 these traces are in direct contacted with the Silver Polymer. On Layers 5, 6 & 7 these traces are "floating" grounds and are of a width that is at least 3 times the thickness of the dielectric material between conductive layers - so as to provide a shield for the cable sides from external EMI in various frequencies. All ground traces are electrically connected to each other through vias in the rigid sections.
Flex Circuit Roadmap
Formed-To-Install Flex Circuit
### Flex Circuit Roadmap

#### Innovations in Support of Drivers

<table>
<thead>
<tr>
<th><strong>Materials Development</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>• Low Dk dielectrics</td>
</tr>
<tr>
<td>• Adhesive-less laminates</td>
</tr>
<tr>
<td>• Shielding alternatives</td>
</tr>
<tr>
<td>• “No Flow” pre-pregs</td>
</tr>
<tr>
<td>• Embedded passive laminates</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Process Development</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>• Selective covercoat bonding</td>
</tr>
<tr>
<td>• Thermal management modeling</td>
</tr>
<tr>
<td>• Layer registration/sequential lamination</td>
</tr>
<tr>
<td>• Impedance modeling</td>
</tr>
</tbody>
</table>
Flex Circuit Roadmap

Summary

• Overseas Competition Creating Price Erosion
  - Low profit margins make IR&D difficult
  - Innovation stifled by less players
  - Potential for comprise of IP

• Materials & Consumables Made Overseas
  - Susceptible to delays and price variances

• Process Equipment Made Overseas
  - Designed for commercial product production

• Lack of Industry Gap Analysis/Road Map
  - No organized R&D effort
IPC Printed Circuit Board
Defense Roadmaps
IPC/DR

Summary and Common Challenges
PCB Technology and Market Migration

• The Market Trend is Obvious
• Certain D&A PCBs are being off-shored
• Defense and Aerospace Companies Must Think of the Long Term Impact on Domestic PCB Industry
  • Reverse ITAR Potential
  • Innovations will be required to compete and retain technological advantage

Let's not forget about PCB consumables
• Laminate Materials
• Chemistry
• Drill Bits
• Equipment

IPC Programs: D&A Technology Roadmap
D&A Task Force
IP Protection Standard
Next Gen PCBs require capital investment and advanced capabilities

- New 24”x36” Hi-Speed LDI Laser Direct Imager
- New 26”x38” Large Format Mod Drill for +/- 0.0005” controlled depth capability and Ultra-Hi Aspect Ratio Drilling
- 3’x5’ Autoclave Microwave/Rf Market, up to 27”x48” panel sizes, and Complex Full-Flex/Rigid-Flex

ASC Econoclave Model EC3X5
Next Gen Products also require improved metrology and automation.

Cu Thickness Measurement Robot -

High Speed VNA

Line Width/Pad Size Measurement Robot (also used for LGA Co-Planarity)

CI-1000 Impedance Robot with SPP in-Process Df Measurement Capability Improves Impedance Tolerance Capability
**Defense Roadmaps Summary**

- DoD needs to be concerned with current PCB market transition
- D&A market will continue to be the focus of NA based fabricators
- Market growth depends on economic climate and government funding
- The domestic PCB industry needs to lobby for retention of this market in NA and to prevent further off-shoring
- Technology demands of D&A PCBs will continue to increase with focus on bandwidth, size and weight reduction
- NA PCB fabricators will need to make capital investments in equipment and infrastructure to support next gen PCBs
- Innovation and IP Protection will be key to retaining competitive edge
Defense Road Maps

Question and Answer